CLAIMS

1. A method for sub-sampling pixelized image data gathered in overlapping blocks (B), including the steps of:

reading, line by line, from an image memory (M1) containing the pixelized image;

accumulating as many lines as provided by the sub-sampling ratio in the vertical direction, using as many groups of accumulators (Aij) as there are blocks in the horizontal image direction and as many accumulators per group as provided by the sub-sampling ratio in the horizontal direction; and

memorizing the accumulated values in as many result memories (MR) as there are accumulator groups, each result memory containing sub-sampled matrixes of a number of blocks corresponding to the number of overlapping blocks in the vertical direction.

2. The method of claim 1, wherein the memorization is performed in an interlaced fashion.

3. The method of claim 1 or 2, consisting of dividing the accumulated values by the product of the sub-sampling ratios in both directions, to obtain average values to be memorized as sub-samples.

4. The method of claim 3, wherein the division of an accumulated value of several lines of the image memory to obtain an average value is obtained by only taking into account a number of most significant bits, smaller than the number of bits of the result value.

5. The method of any of claims 1 to 4, wherein the lines of the image memory (M1) are read successively from the first one for a number of lines corresponding to the sub-sampling ratio in the vertical direction, after which the first following line and a previously-used line are alternately read.

6. A circuit for sub-sampling pixelized image data distributed in overlapping blocks (B), including:

a number of adders (Sij) corresponding to the number of result block pixels in a first direction, multiplied by the number of blocks in a second direction;

a number of accumulators (Aij) identical to the number of adders; and

a number of result memories (MR) of the sub-sampled values corresponding to the number of blocks in the first direction.

7. The circuit of claim 6, wherein the accumulators (Aij) are controllable for addition or subtraction of a current value to the previously-accumulated result.

8. The circuit of claim 6 or 7, wherein the number of inputs of each adder corresponds to the sub-sampling ratio in the first direction.

9. The circuit of any of claims 6 to 8, wherein said result memories (MR) include a number of lines corresponding to the number of blocks in the second direction, multiplied by the number of pixels of the result blocks in the second direction.

10. The circuit of any of claims 6 to 9, wherein the number of bits of a result value stored in one of said result memories is smaller than the number of bits of the values of the pixelized image data, the difference between the two numbers of bits defining the division ratio for obtaining the average value of the pixels of each sub-sampled group.